Influence of the Reduction Order in Multiplier Verification using Computer Algebra

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Bugs in hardware are expensive!

Challenge: Multiplication

System

Model

Specification

Preprocessing eliminates internal nodes of full- and half-adders. Specification is reduced by the rewritten gate polynomials.

Polynomial reduction orderings:

Simple Multiplier

Complex Multiplier

Final stage adder:
Ripple-Carry adder

PP accumulation:
Array

PP generation:
AND Gates

Final stage adder:
Ripple-Carry adder

PP accumulation:
Wallace-Tree

PP generation:
Booth Encoding

Preprocessing eliminates internal nodes of full- and half-adders. Specification is reduced by the rewritten gate polynomials.