COLUMNS vs. ROWS

Influence of the Reduction Order in Multiplier Verification using Computer Algebra

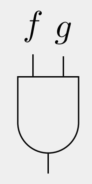
Daniela Kaufmann
fmv.jku.at/kaufmann

Computer Algebra

Bugs in hardware are expensive!
Challenge: Multiplication

System

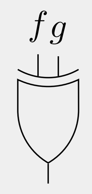
AND-Gate $f \wedge g = y$



f	g	y
0	0	0
0	1	0
1	0	0
1	1	1

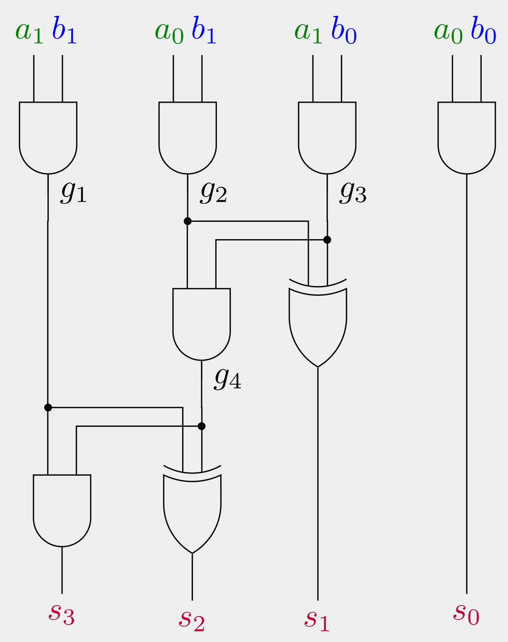
$y = fg$

XOR-Gate $f \oplus g = y$



f	g	y
0	0	0
0	1	1
1	0	1
1	1	0

$y = f + g - 2fg$



Model

$$
\begin{array}{rl}
s_3 = g_1 \wedge g_4 & -s_3 + g_1 g_4, \\
s_2 = g_1 \oplus g_4 & -s_2 - 2g_4 g_1 + g_4 + g_1, \\
g_4 = g_2 \wedge g_3 & -g_4 + g_2 g_3, \\
s_1 = g_2 \oplus g_3 & -s_1 - 2g_2 g_3 + g_2 + g_3, \\
g_1 = a_1 \wedge b_1 & -g_1 + a_1 b_1, \\
g_2 = a_0 \wedge b_1 & -g_2 + a_0 b_1, \\
g_3 = a_1 \wedge b_0 & -g_3 + a_1 b_0, \\
s_0 = a_0 \wedge b_0 & -s_0 + a_0 b_0, \\
a_1 \in \mathbb{B} & -a_1^2 + a_1, \\
a_0 \in \mathbb{B} & -a_0^2 + a_0, \\
b_1 \in \mathbb{B} & -b_1^2 + b_1, \\
b_0 \in \mathbb{B} & -b_0^2 + b_0
\end{array}
$$

Specification

$$(2a_1 + a_0) * (2b_1 + b_0) = 8s_3 + 4s_2 + 2s_1 + s_0$$

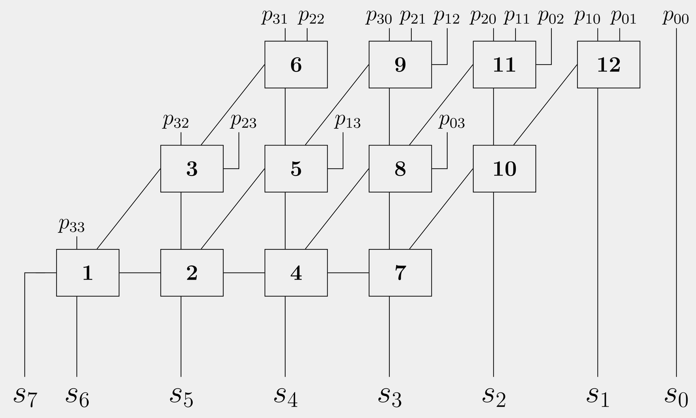
Reduction

$$
\begin{array}{r}
8s_3 + 4s_2 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0 \\
4s_2 + 8g_4g_1 + 2s_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0 \\
4g_4 + 2s_1 + 4g_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0 \\
2s_1 + 4g_2g_3 + 4g_1 + s_0 - 4a_1b_1 - 2a_1b_0 - 2a_0b_1 - a_0b_0 \\
\vdots \\
0
\end{array}
$$

Reduction Order

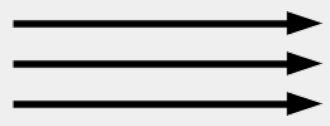
Preprocessing eliminates internal nodes of full- and half-adders.
Specification is reduced by the rewritten gate polynomials.

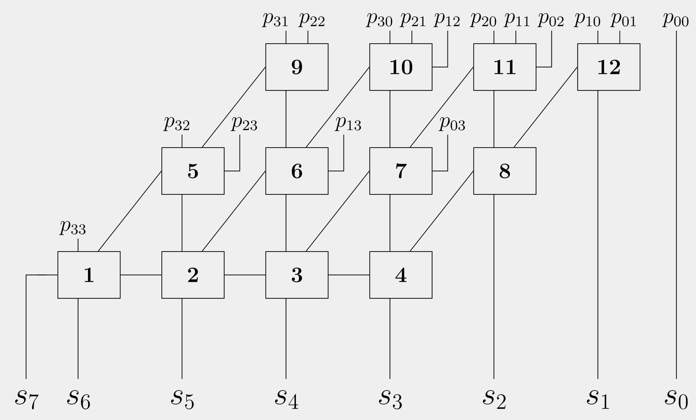
Polynomial reduction orderings:

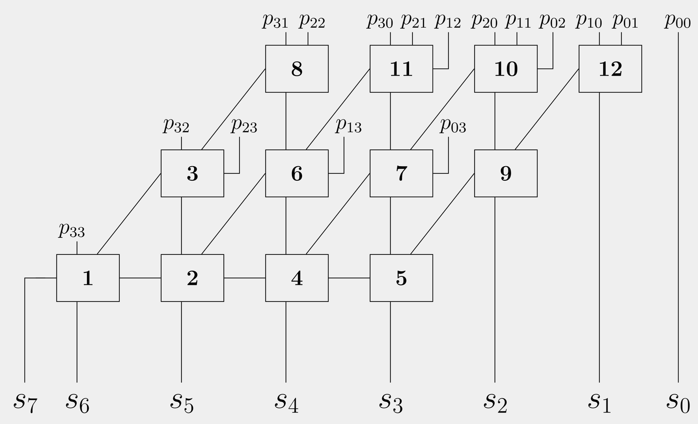


Column-wise Order

Row-wise Order

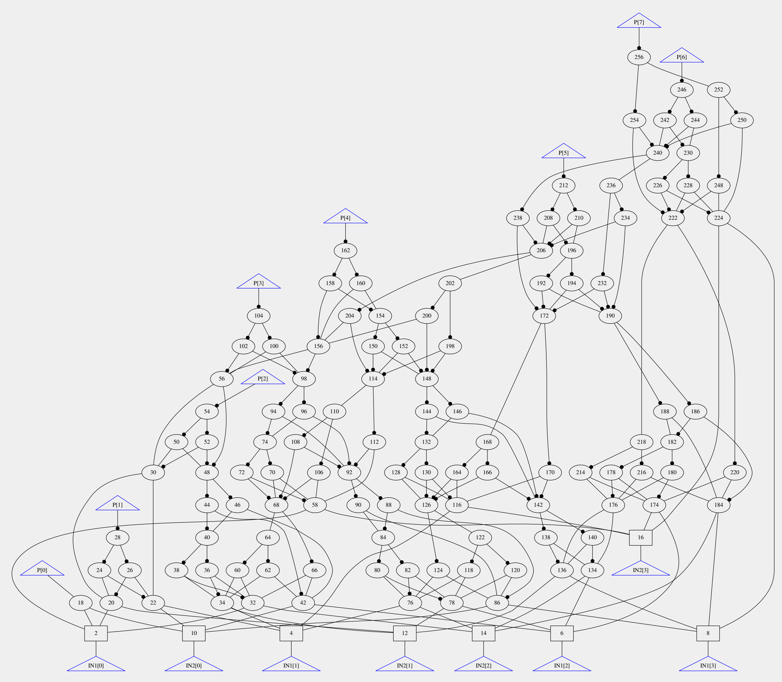






Arbitrary reverse topological

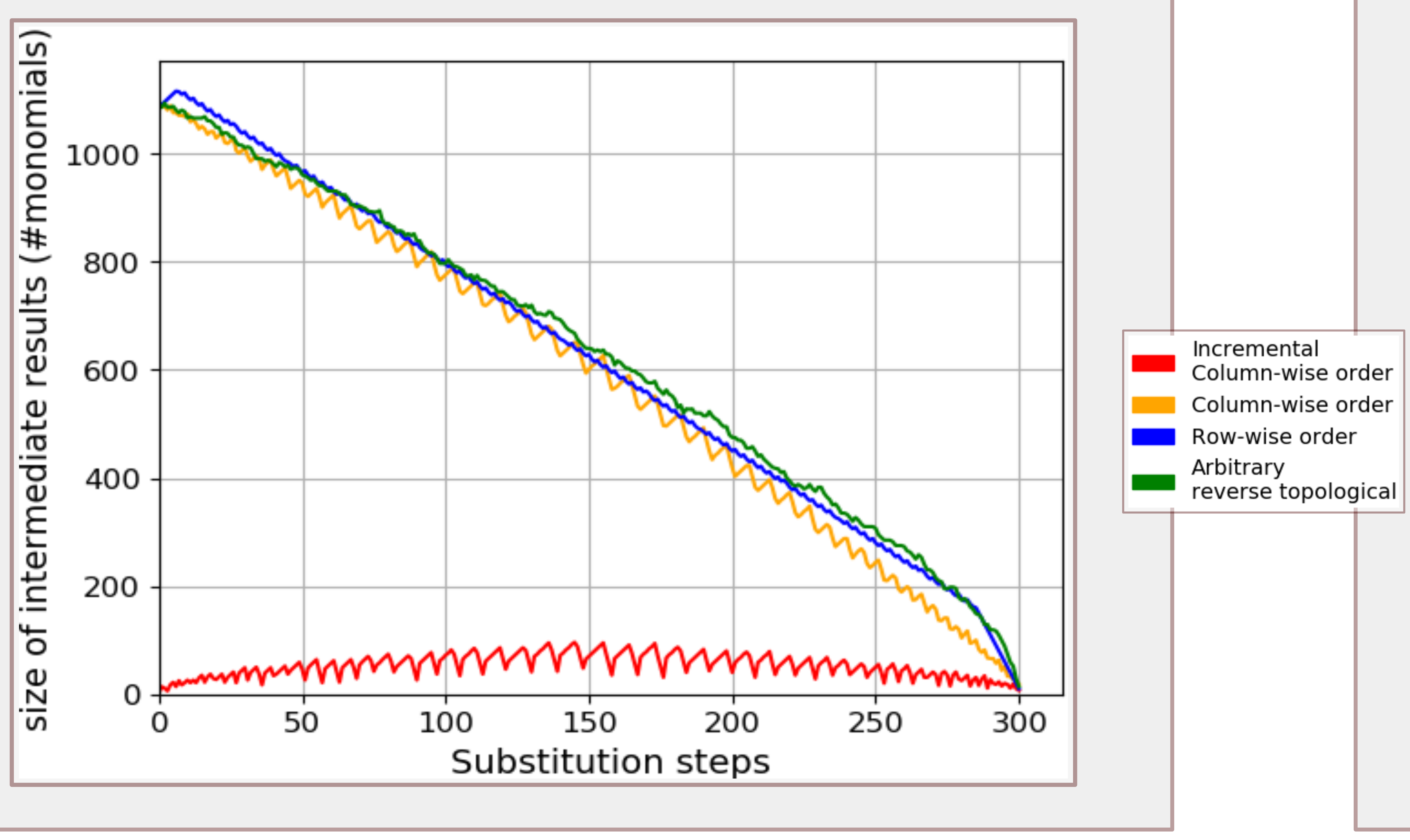
Simple Multiplier



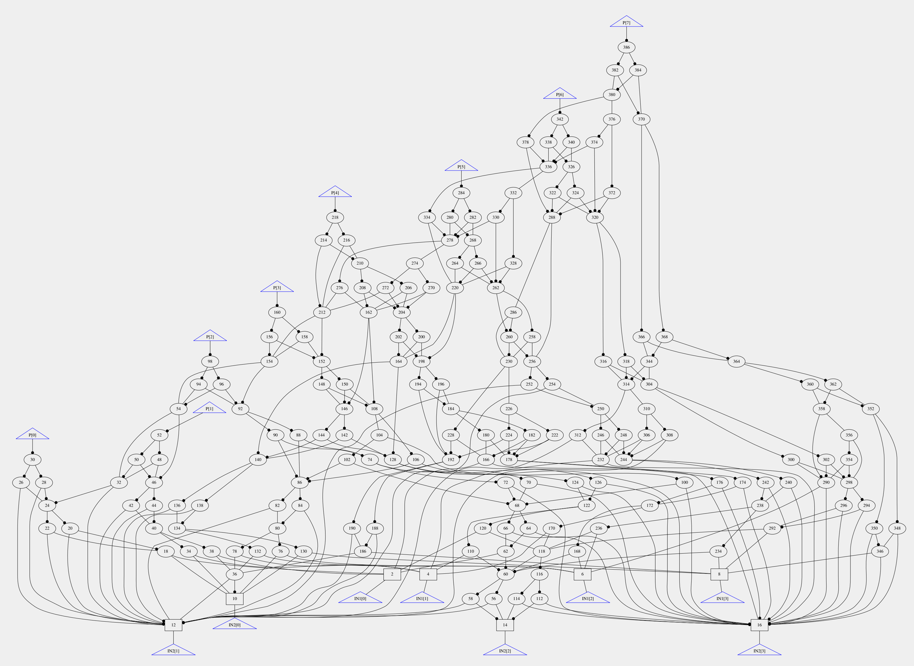
Final stage adder:
Ripple-Carry adder

PP accumulation:
Array

PP generation:
AND Gates



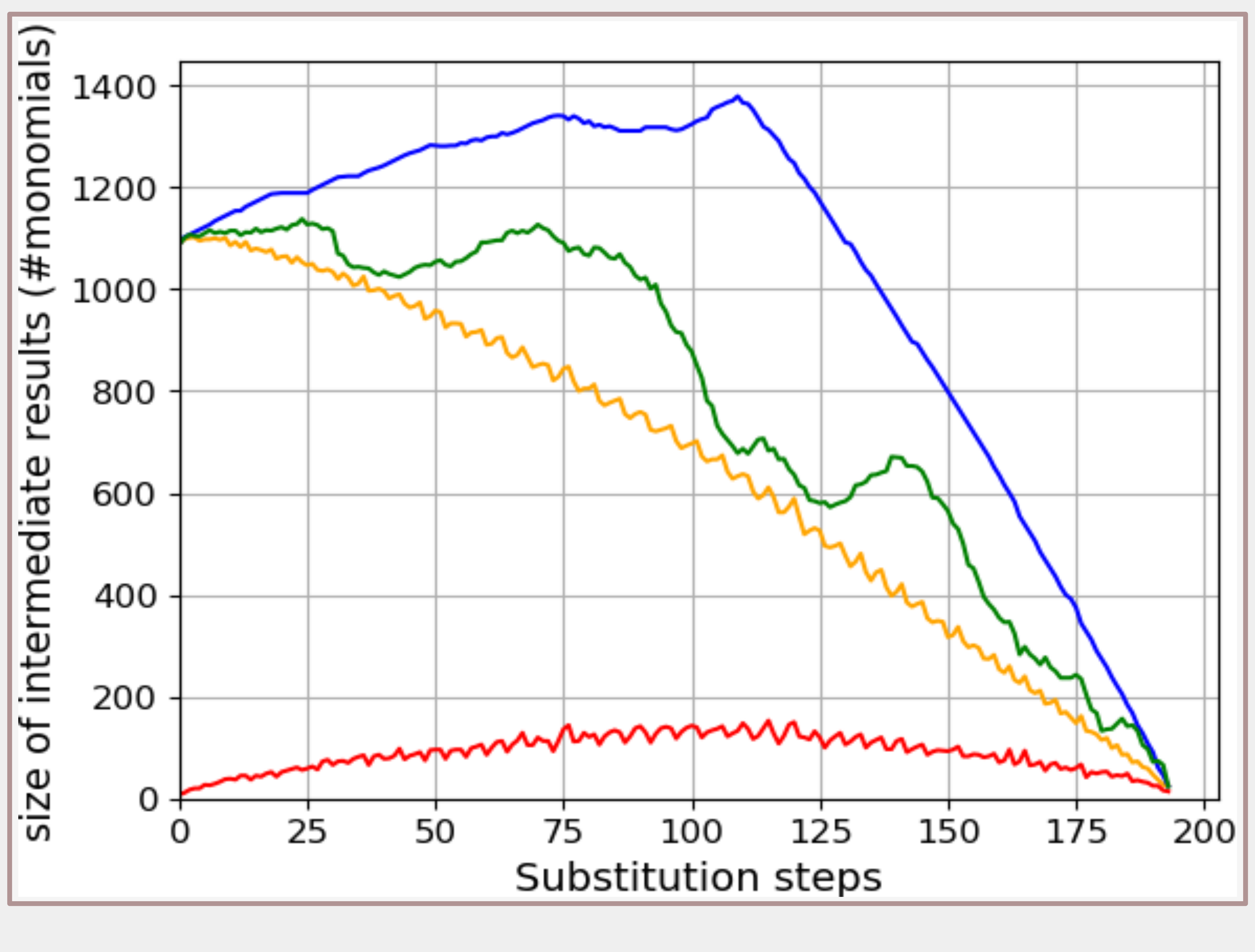
Complex Multiplier



Final stage adder:
Ripple-Carry adder

PP accumulation:
Wallace-Tree

PP generation:
Booth Encoding



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