CATEGORICAL SEMANTICS OF DIGITAL CIRCUITS

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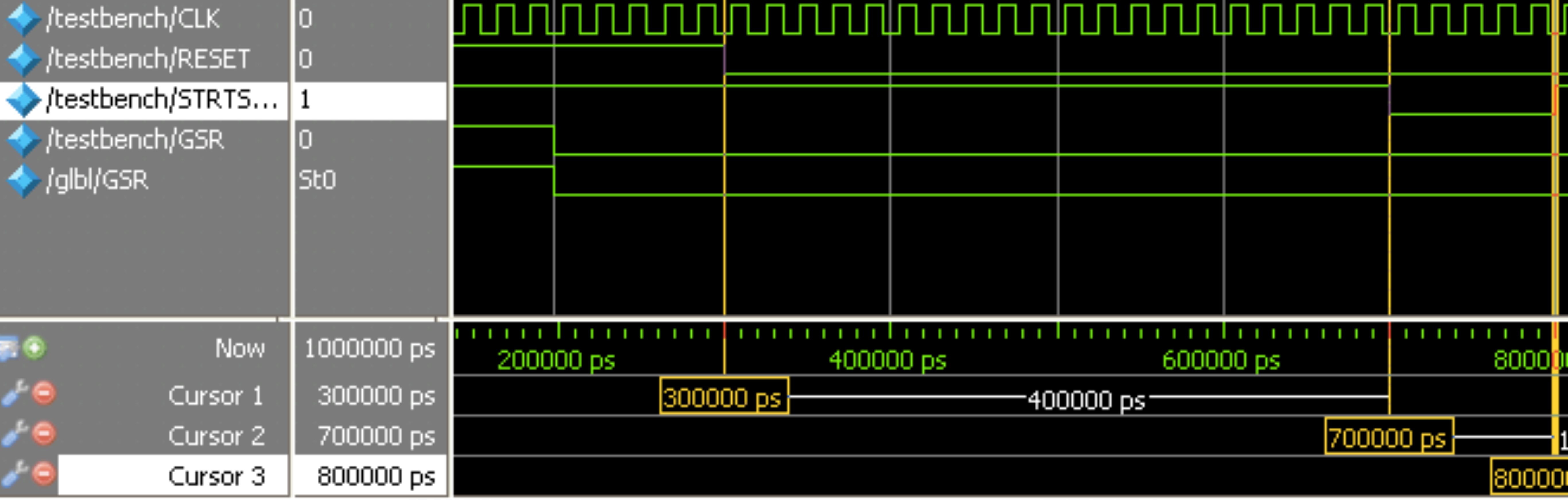
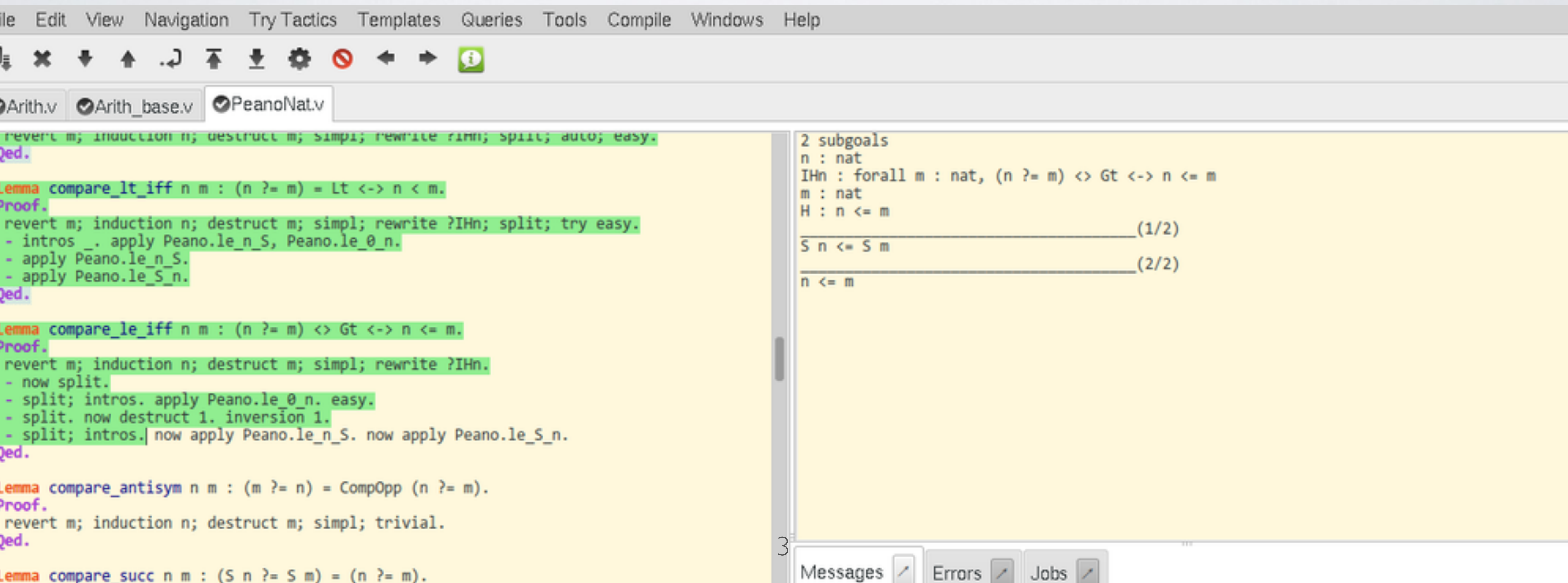
UNIVERSITY OF BIRMINGHAM

GOS The Geometry of Synthesis

VERITYGOS.ORG


/testbench/CLK
/testbench/RESET
/testbench/STRTS...
/testbench/GSR
/glbl/GSR
0
0
1
0
St0
Now
Cursor 1
Cursor 2
Cursor 3
1000000 ps
300000 ps
700000 ps
800000 ps
200000 ps
400000 ps
600000 ps
300000 ps
400000 ps
700000 ps

vs

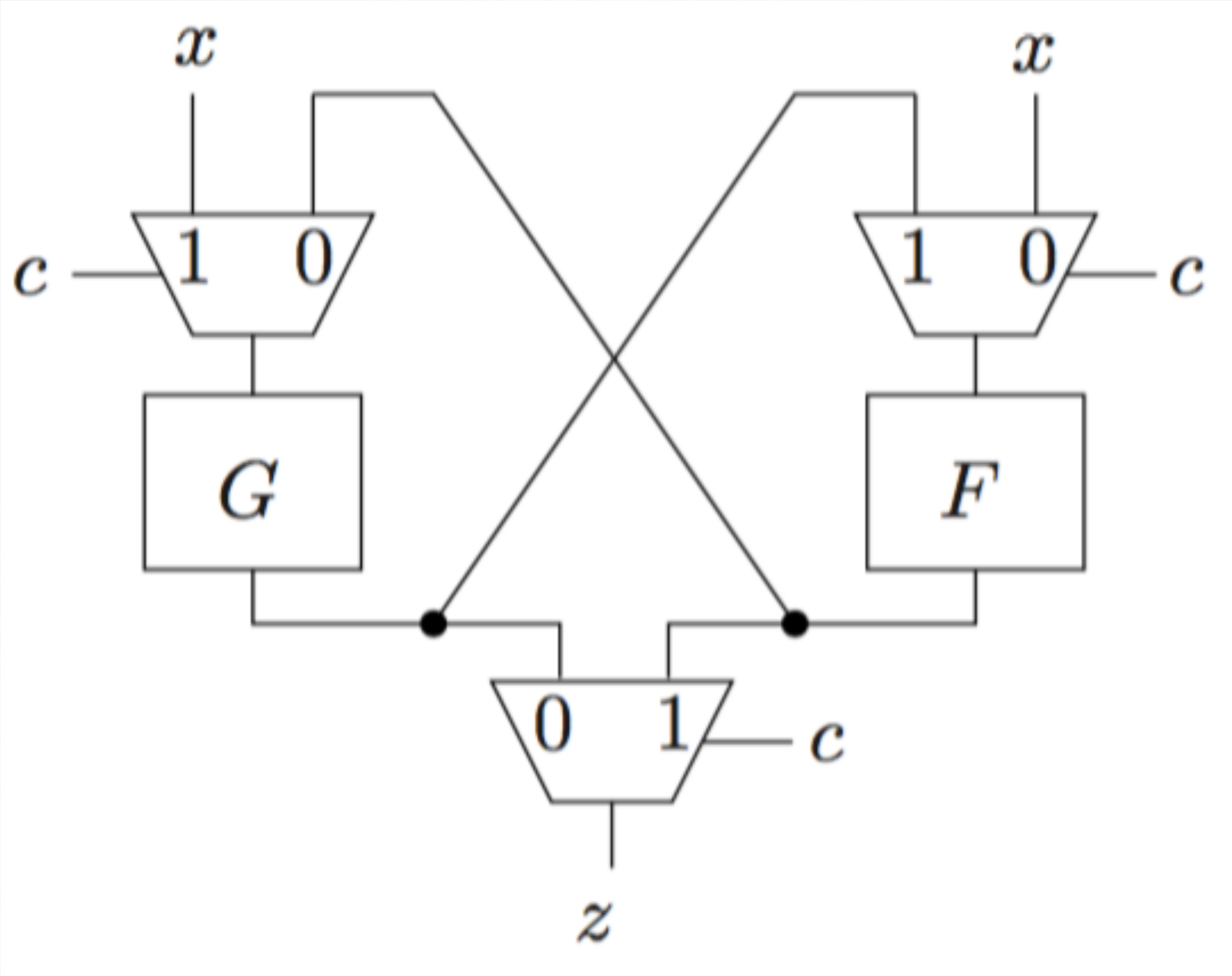

Edit View Navigation Try Tactics Templates Queries Tools Compile Windows Help
Arith.v
Arith_base.v
PeanoNat.v
Lemma compare_lt_iff n m : (n ?= m) = Lt <-> n < m.
Proof.
revert m; induction n; destruct m; simpl; rewrite ?IHn; split; try easy.
- intros _. apply Peano.le_n_S, Peano.le_0_n.
- apply Peano.le_n_S.
- apply Peano.le_S_n.
Qed.
Lemma compare_le_iff n m : (n ?= m) <> Gt <-> n <= m.
Proof.
revert m; induction n; destruct m; simpl; rewrite ?IHn.
- now split.
- split; intros. apply Peano.le_0_n. easy.
- split. now destruct 1. inversion 1.
- split; intros. now apply Peano.le_n_S. now apply Peano.le_S_n.
Qed.
Lemma compare_antisym n m : (m ?= n) = CompOpp (n ?= m).
Proof.
revert m; induction n; destruct m; simpl; trivial.
Qed.
2 subgoals
n : nat
IHn : forall m : nat, (n ?= m) <> Gt <-> n <= m
m : nat
H : n <= m
(1/2)
S n <= S m
(2/2)
n <= m
Messages
Errors
Jobs

BENEFITS OF SYNTACTIC REASONING

- formalisation
- soundness and completeness not an issue
- robustness to changes
- manipulating open terms
- partial evaluation // supercompilation
- symbolic execution // abstract interpretation
- success story in PLs: operational semantics // types // logics

CAN WE REASON
EQUATIONALLY
SYNTACTICALLY
OPERATIONALLY
ABOUT CIRCUITS?

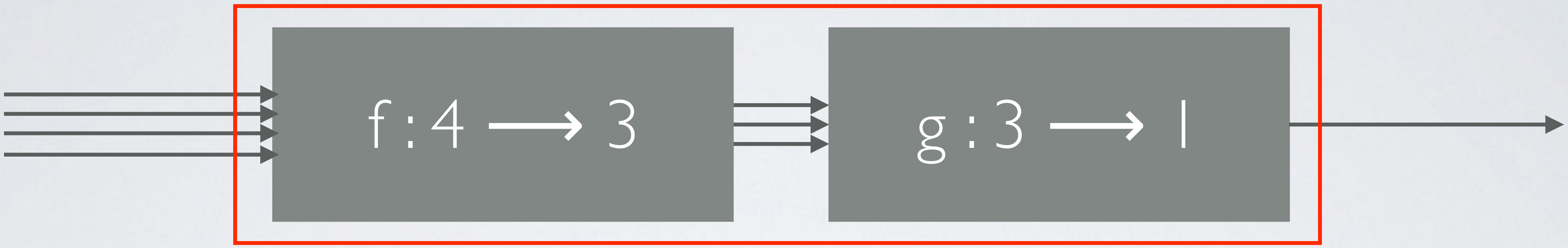
COMBINATIONAL FEEDBACK



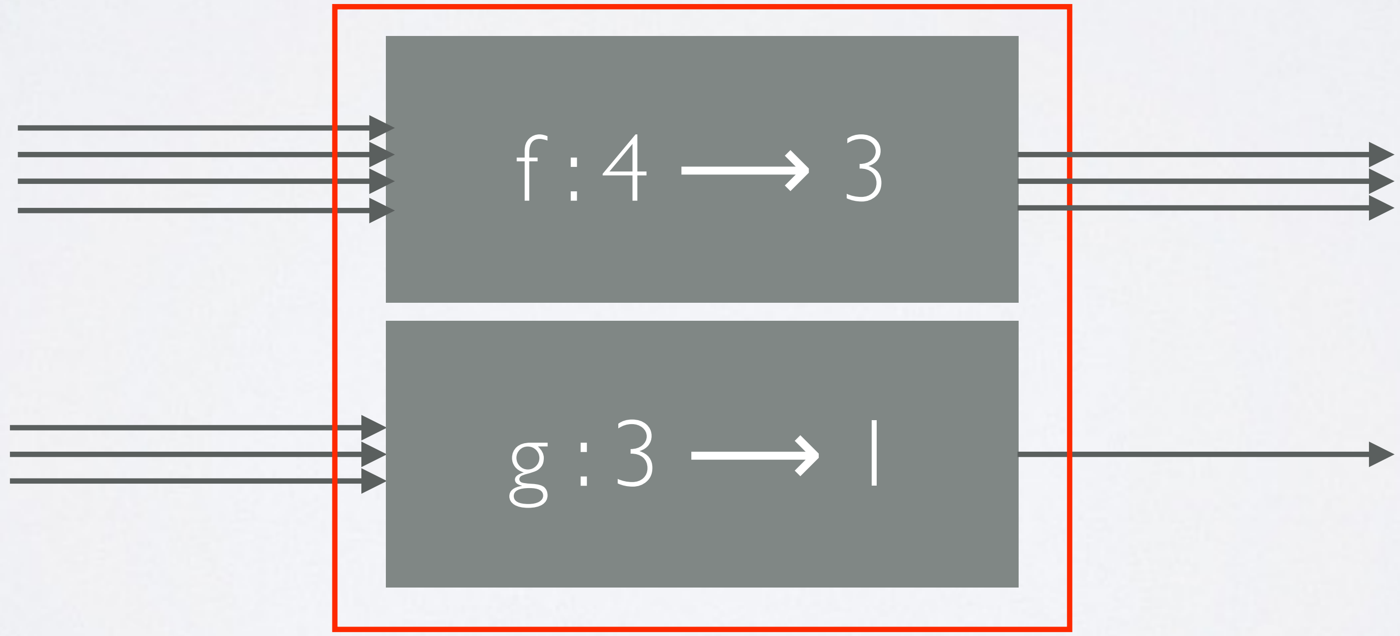
if c **then** F(G(x)) **else** G(F(x))

"PROPS"

COMPOSITION



$f \cdot g : 4 \longrightarrow 1$



$f \otimes g : 7 \longrightarrow 4$

SOUND AND COMPLETE AXIOMS:

STRICT SYMMETRIC TRACED MONOIDAL CATEGORY

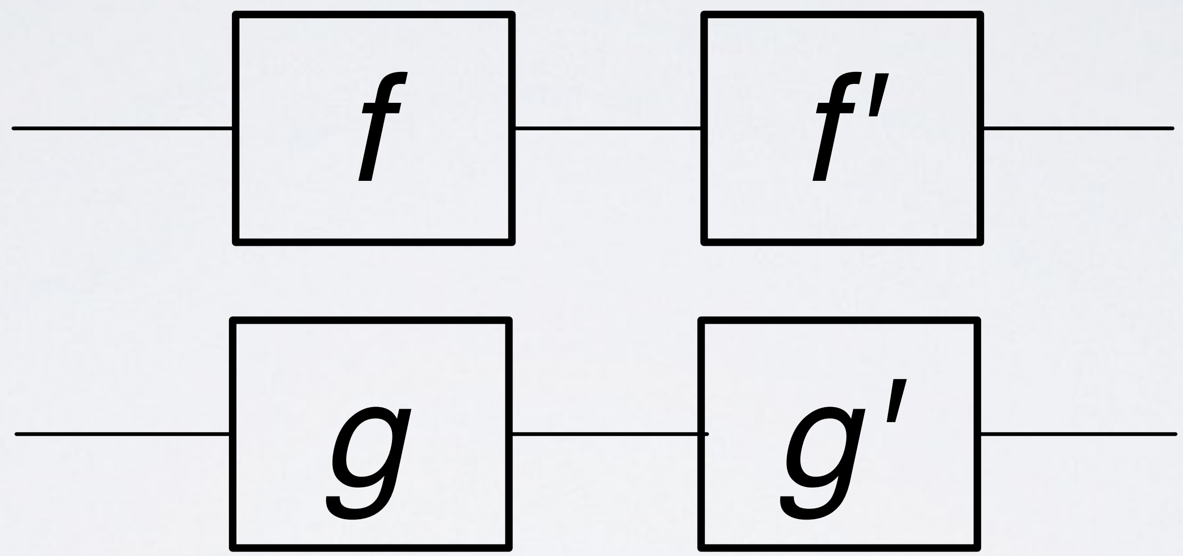
=

DIAGRAMS WITH FEEDBACK
(UP TO TOPOLOGICAL ISOMORPHISM)

=

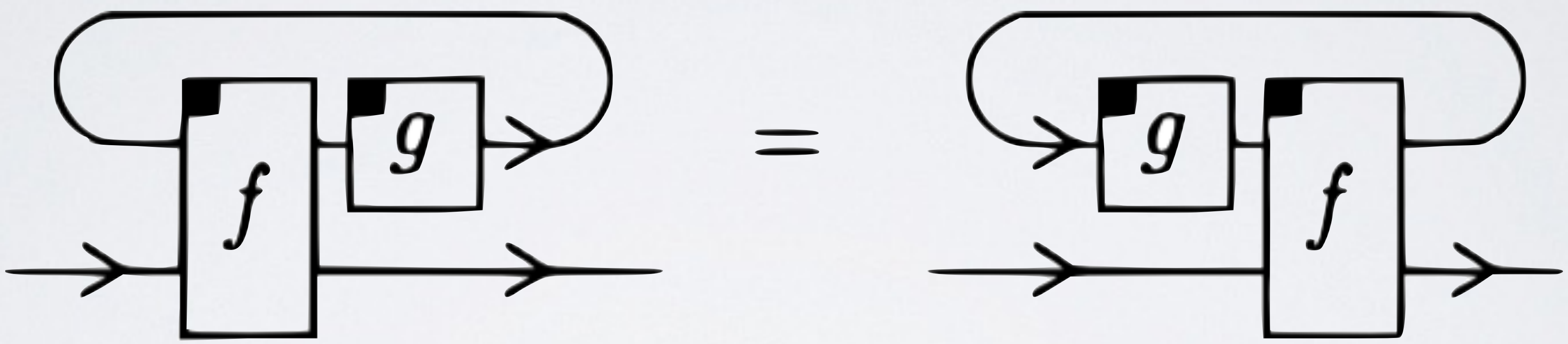
EQUATIONAL FRAMEWORK
FOR CIRCUITS (NETLIST)

EXAMPLE OF EQUATION



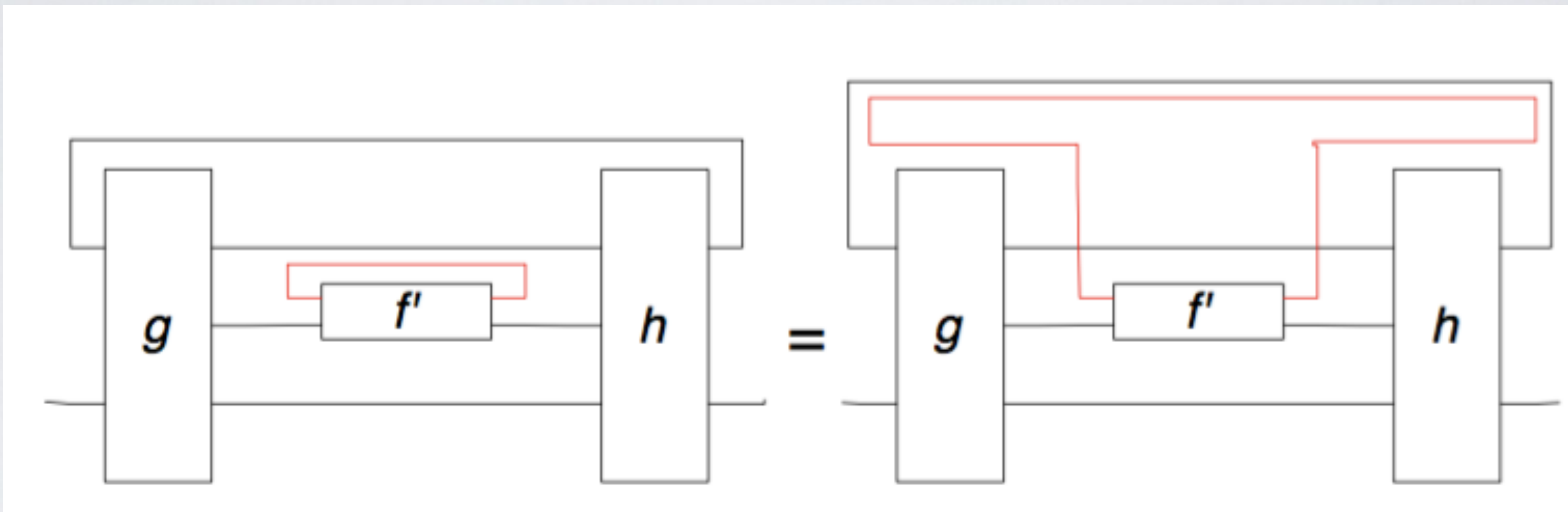
$$(f \cdot f') \otimes (g \cdot g') = (f \otimes g) \cdot (f' \otimes g')$$

EXAMPLE OF EQUATION



$$\mathrm{Tr}(f \cdot (g \otimes n)) = \mathrm{Tr}((g \otimes m) \cdot f)$$

EXAMPLE OF PROPOSITION

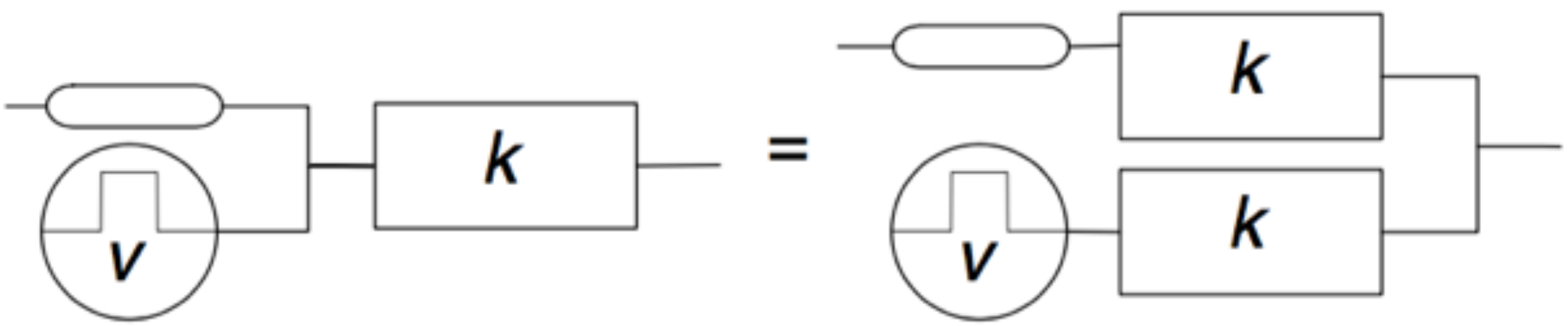


$$\mathrm{Tr}^q\big(g \cdot (m \otimes \mathrm{Tr}^p(f') \otimes n) \cdot h\big) = \mathrm{Tr}^{p+q}\big((p \otimes g) \cdot (\mathsf{x}_{p,m} \otimes r) \cdot f' \cdot (\mathsf{x}_{m,p} \otimes r) \otimes n) \cdot (p \otimes h)\big)$$

Equational $\Longleftrightarrow$ Diagrammatic

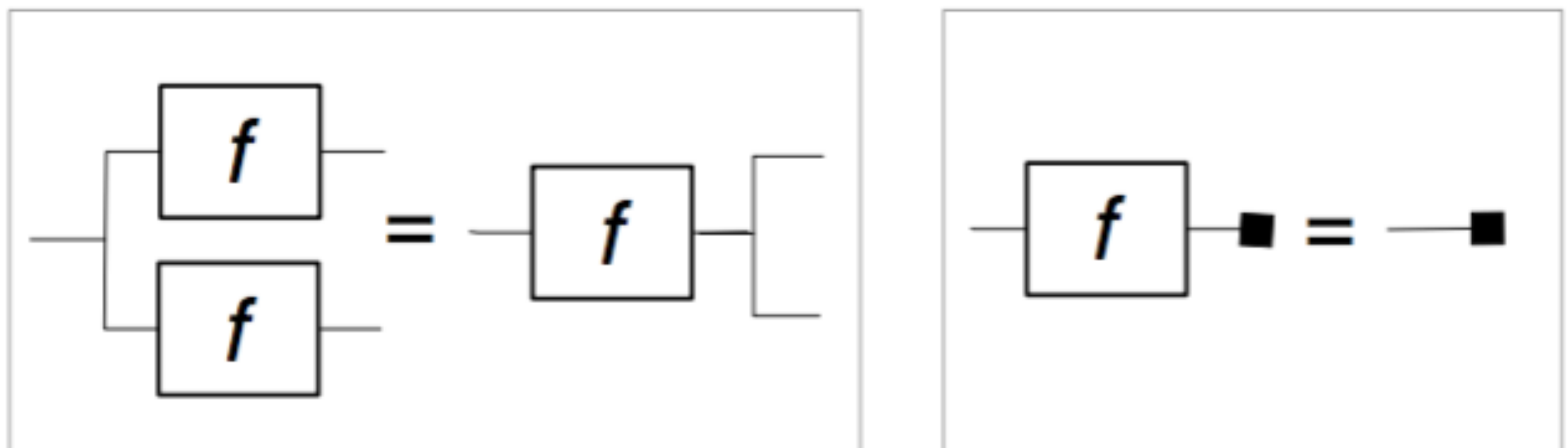
SMALL AXIOMS

Streaming: *For any levels* $\mathbf{v} = v \otimes v'$ *and gate* k, $(\delta^2 \otimes \mathbf{v}) \cdot \nabla_2 \cdot k = ((\delta^2 \cdot k) \otimes (\mathbf{v} \cdot k)) \cdot \nabla_1$.



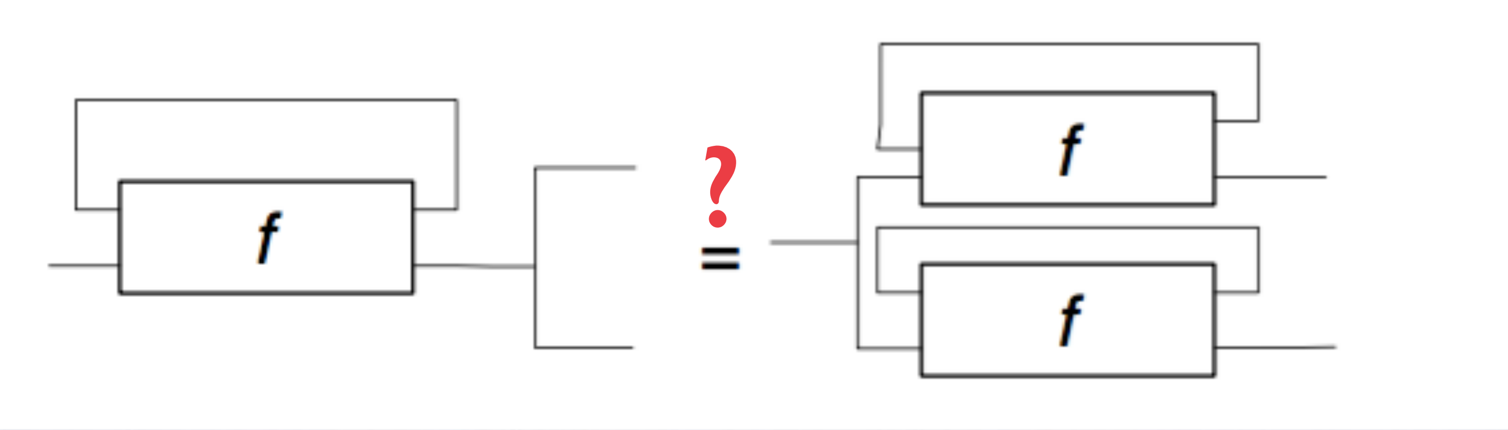
PRODUCT : KEY PROPERTY

$\forall$f.



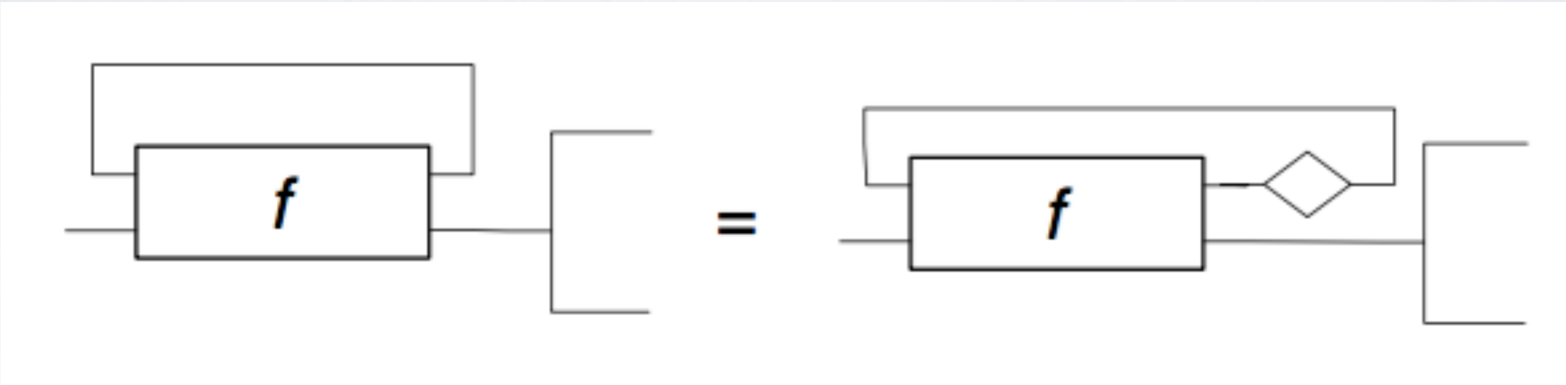
$$\langle f, f\rangle = \Delta_n \cdot (f \otimes f) = f \cdot \Delta_m \qquad f \cdot \mathsf{w}^m = \mathsf{w}^m.$$

DIAGRAMMATIC PROOF



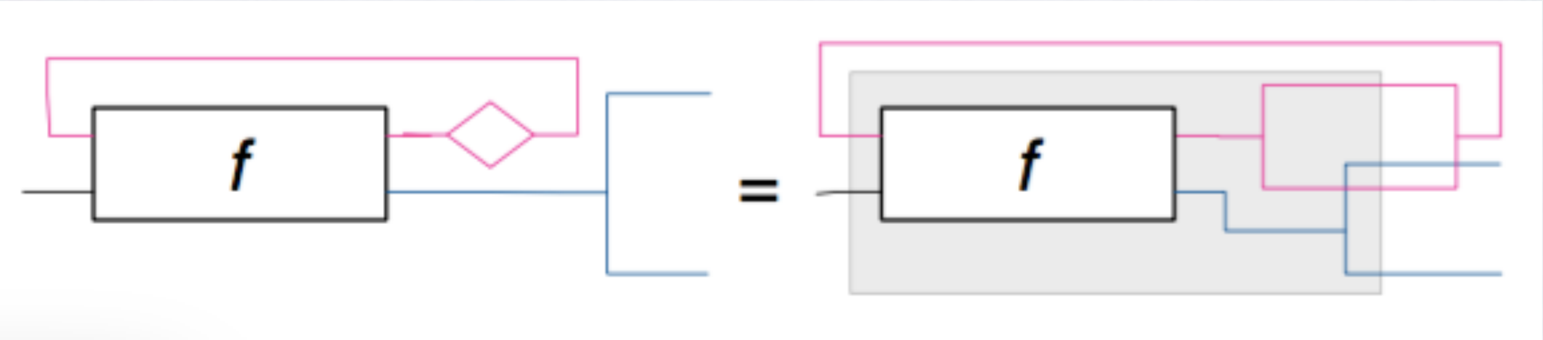
induction

DIAGRAMMATIC PROOF



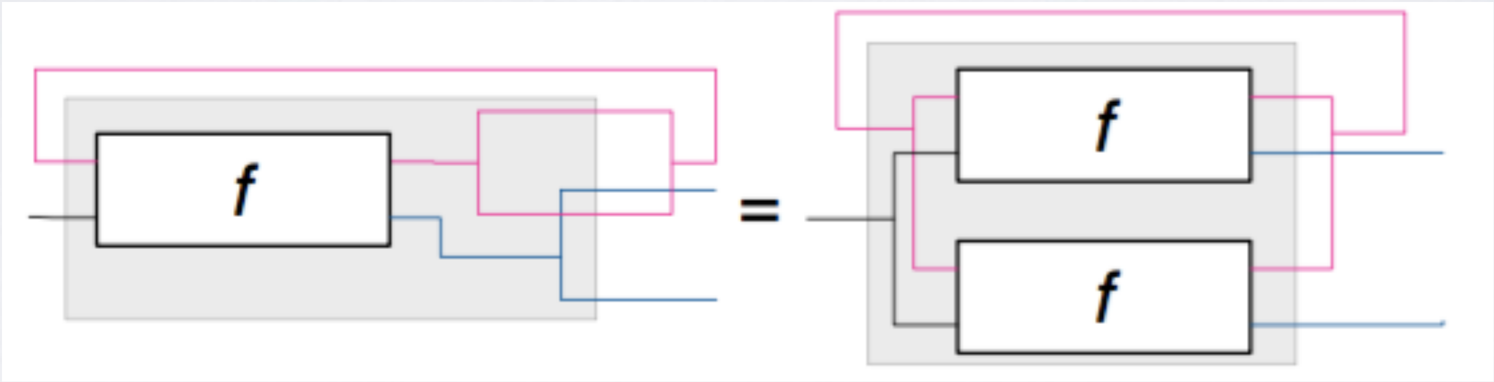
$f \cdot j = 1$

DIAGRAMMATIC PROOF



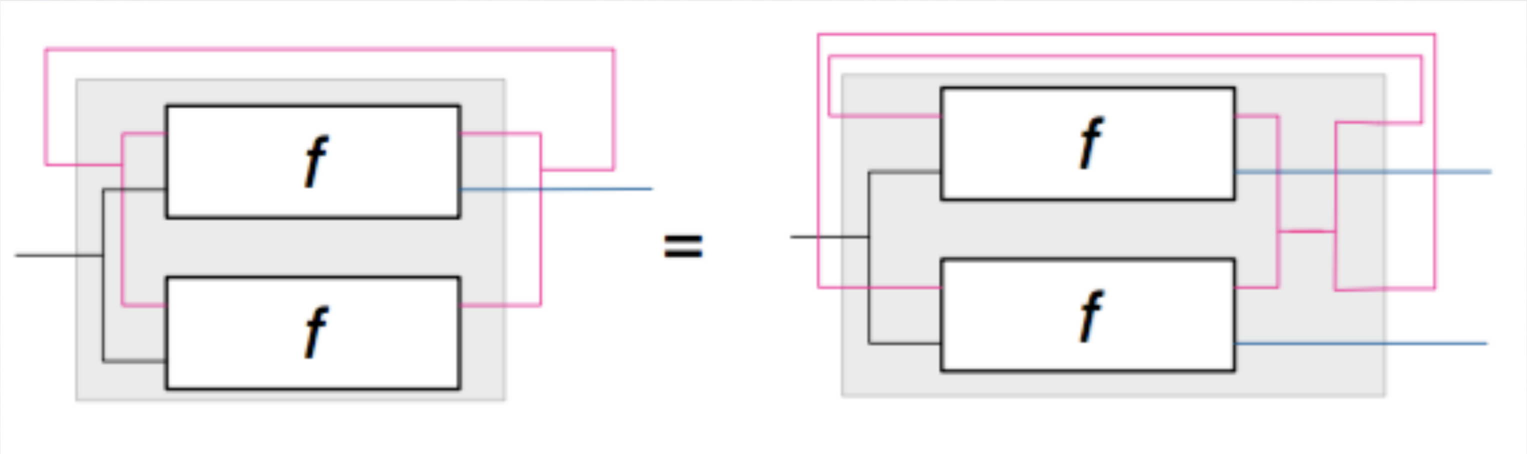
diagrammatic reasoning

DIAGRAMMATIC PROOF



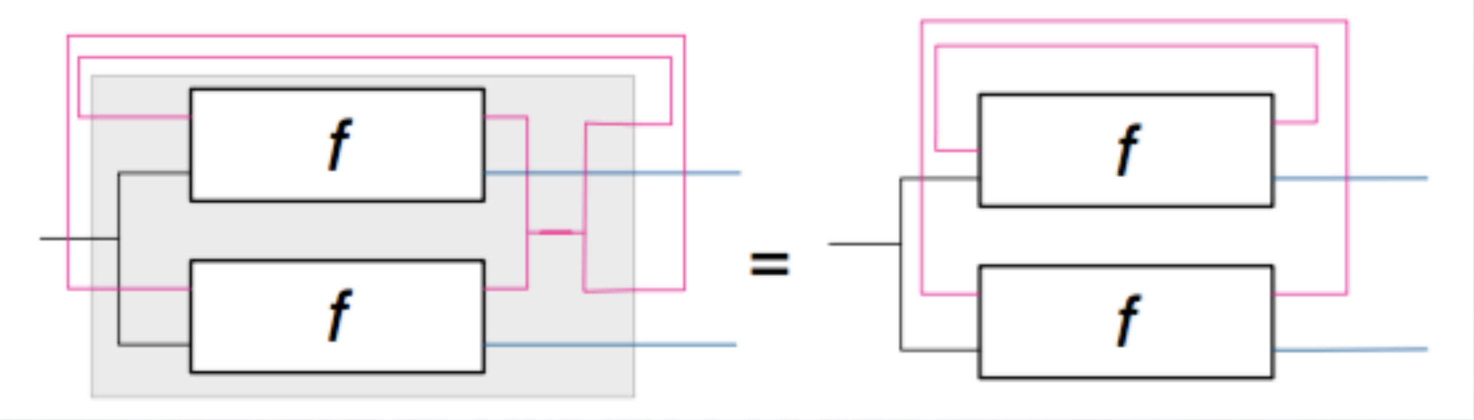
induction hypothesis

DIAGRAMMATIC PROOF



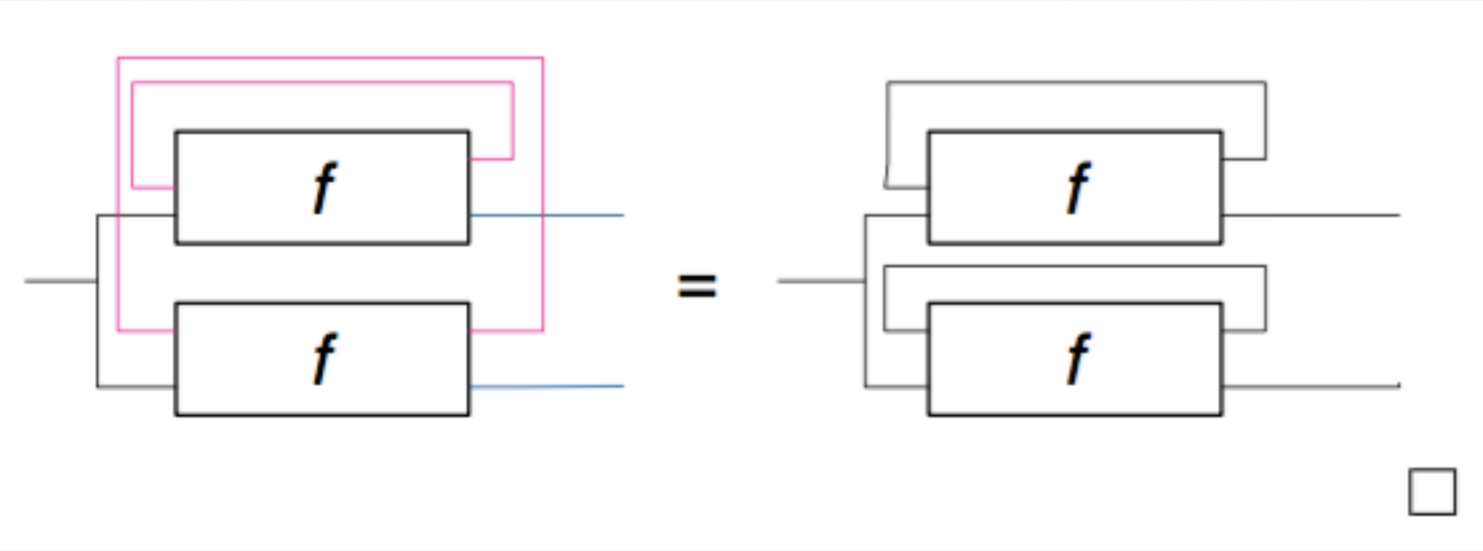
diagrammatic reasoning

DIAGRAMMATIC PROOF



lemma

DIAGRAMMATIC PROOF

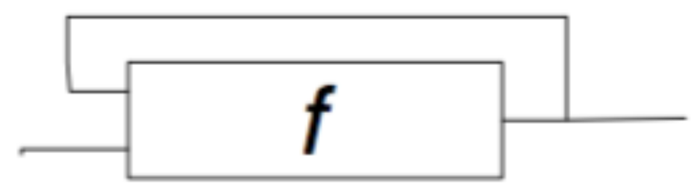


diagrammatic reasoning

EQUATIONS ⇒ SPECS

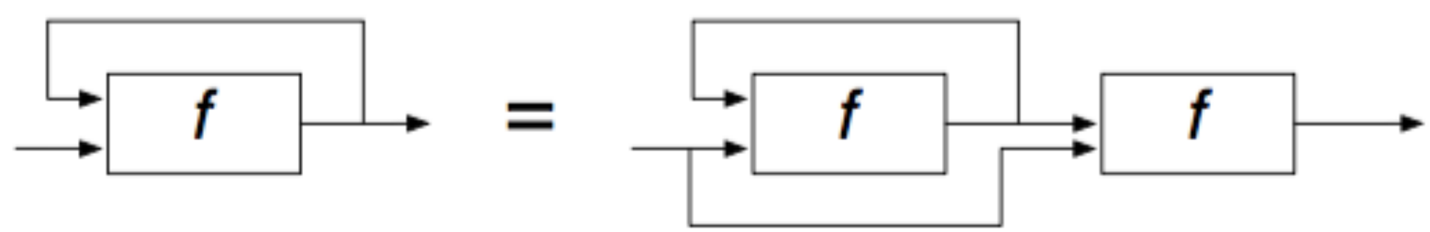
DIAGRAMS ⇒ CALCULATIONS

FEEDBACK + PRODUCT = "*CONTROL-FLOW*" ITERATION



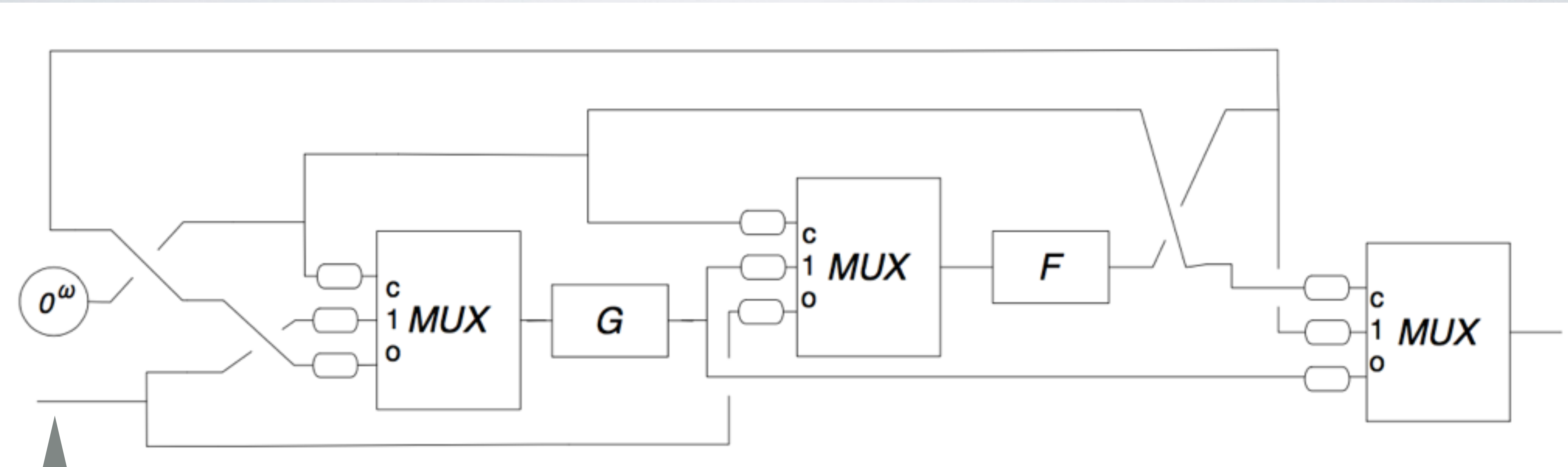
$$\mathrm{iter}^n(f) = \mathrm{Tr}^n(f \cdot (\Delta_n \otimes n)) : m \to n$$

Iteration: $\mathrm{iter}(f) = \langle m, \mathrm{iter}(f)\rangle \cdot f$



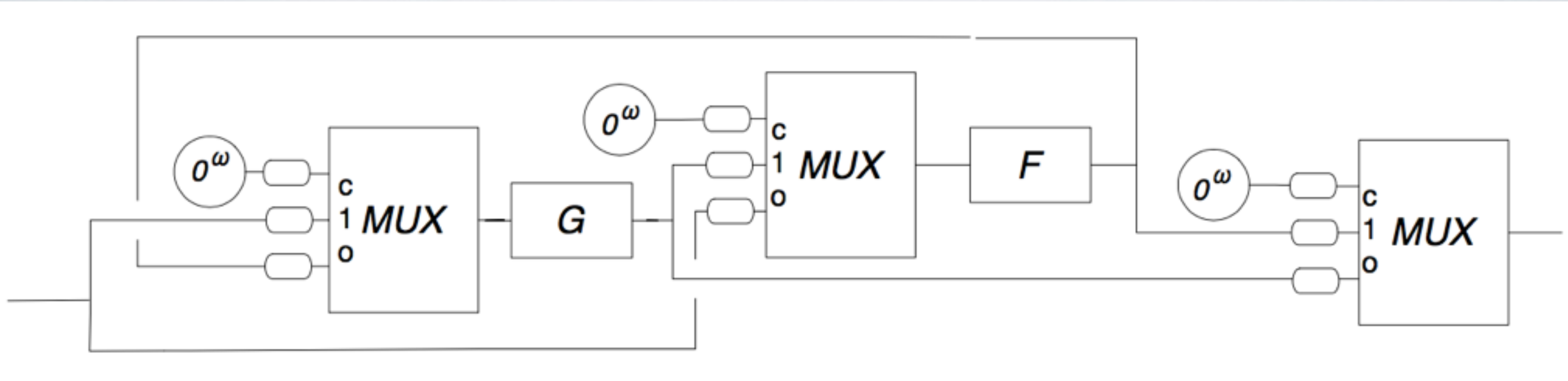
Cazanescu and G. Stefanescu 1990

COMBINATIONAL FEEDBACK

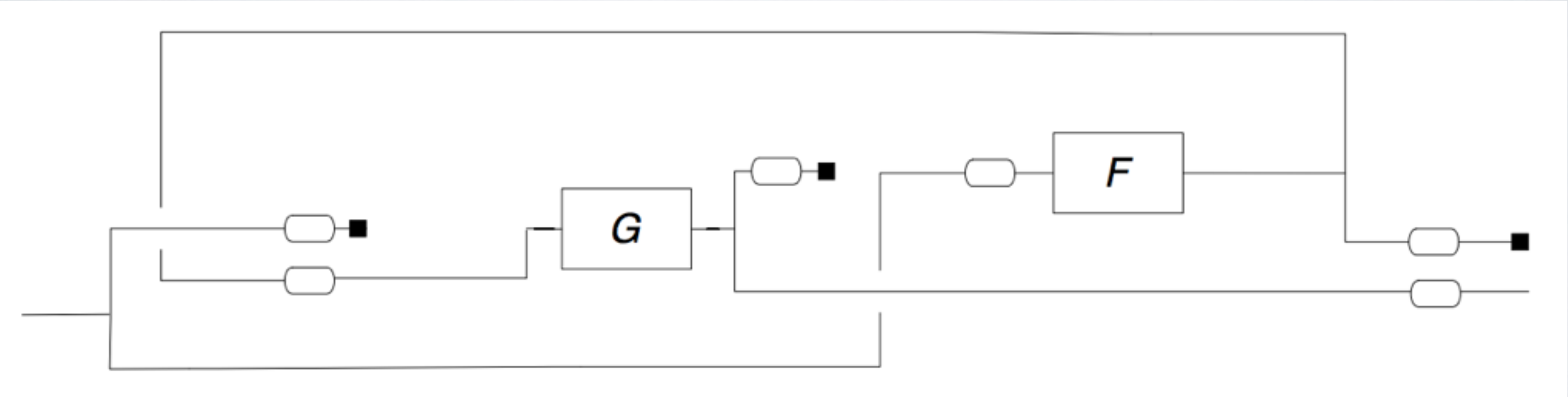


open

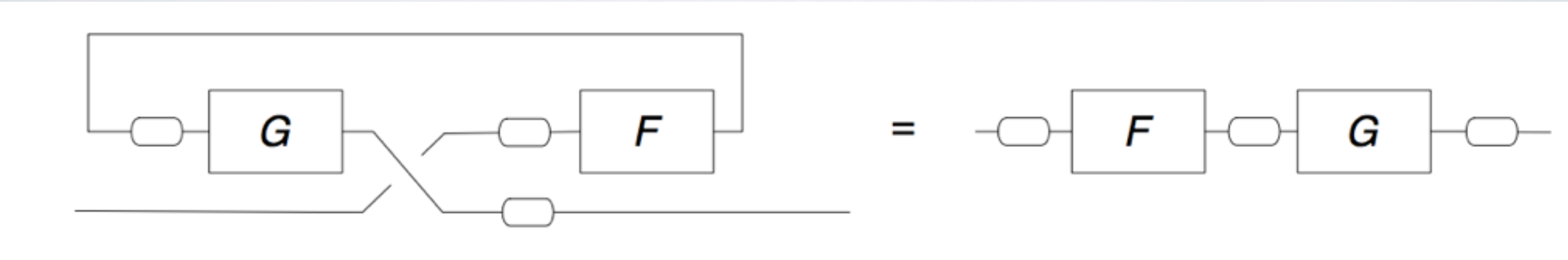
COMBINATIONAL FEEDBACK



COMBINATIONAL FEEDBACK

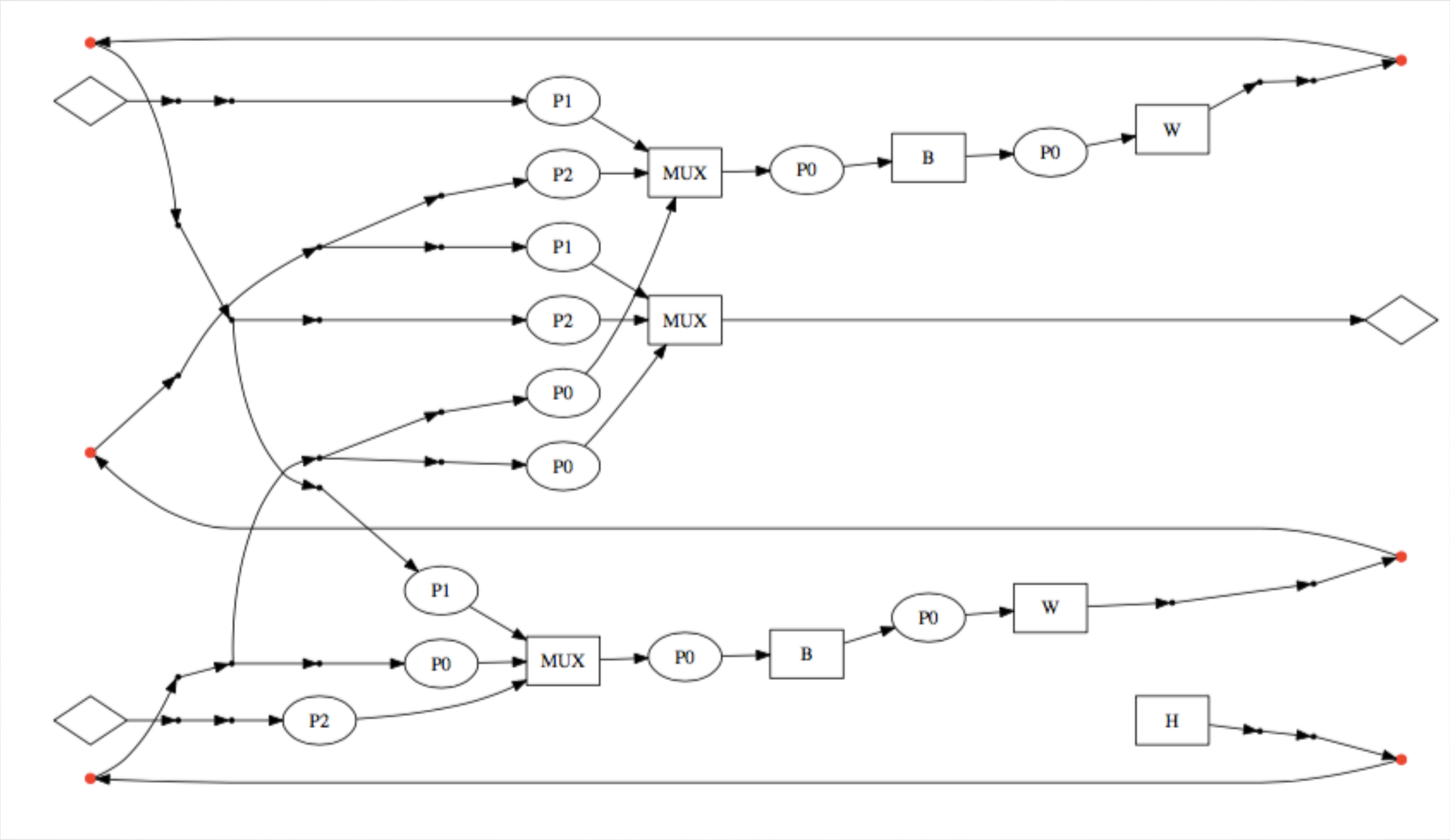


COMBINATIONAL FEEDBACK



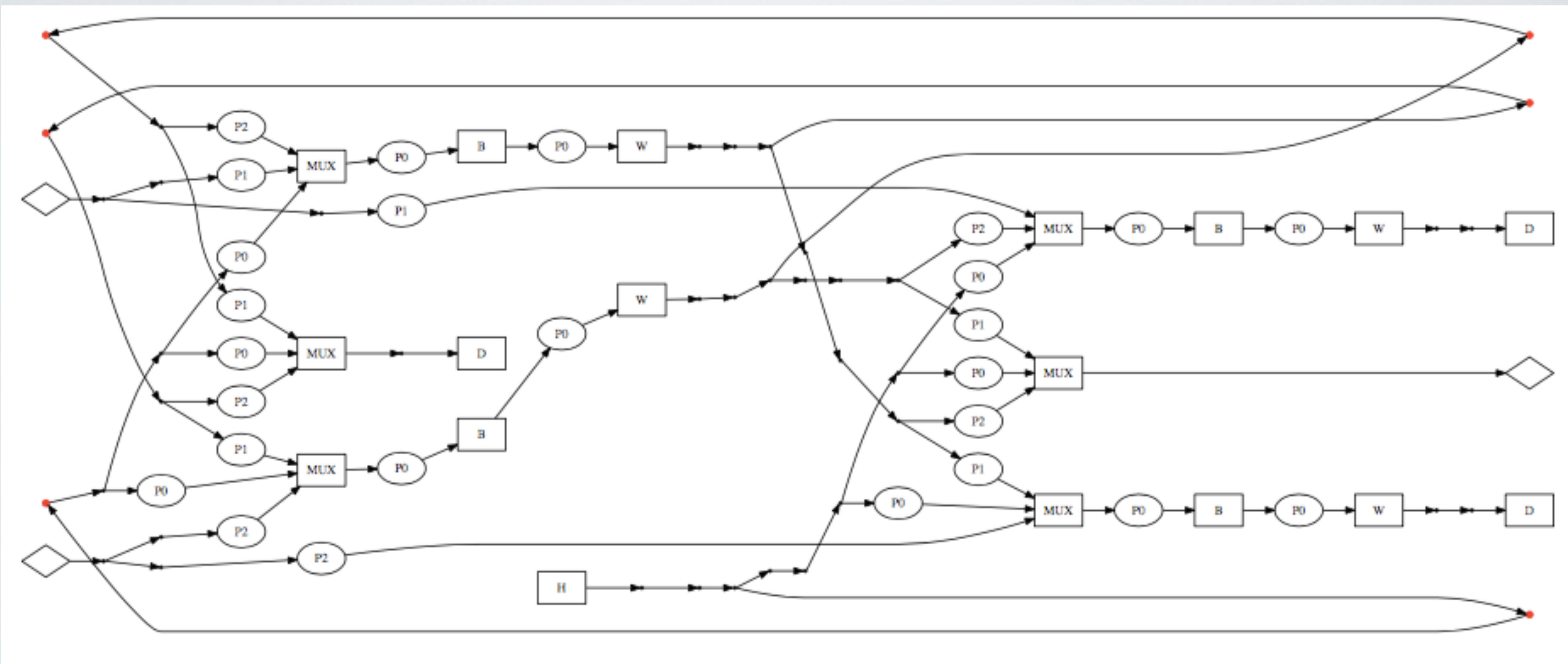
Obs: Unmatched delays lead to different behaviour (as they should).

GRAPH REWRITE



(submitted for publication)

GRAPH REWRITE



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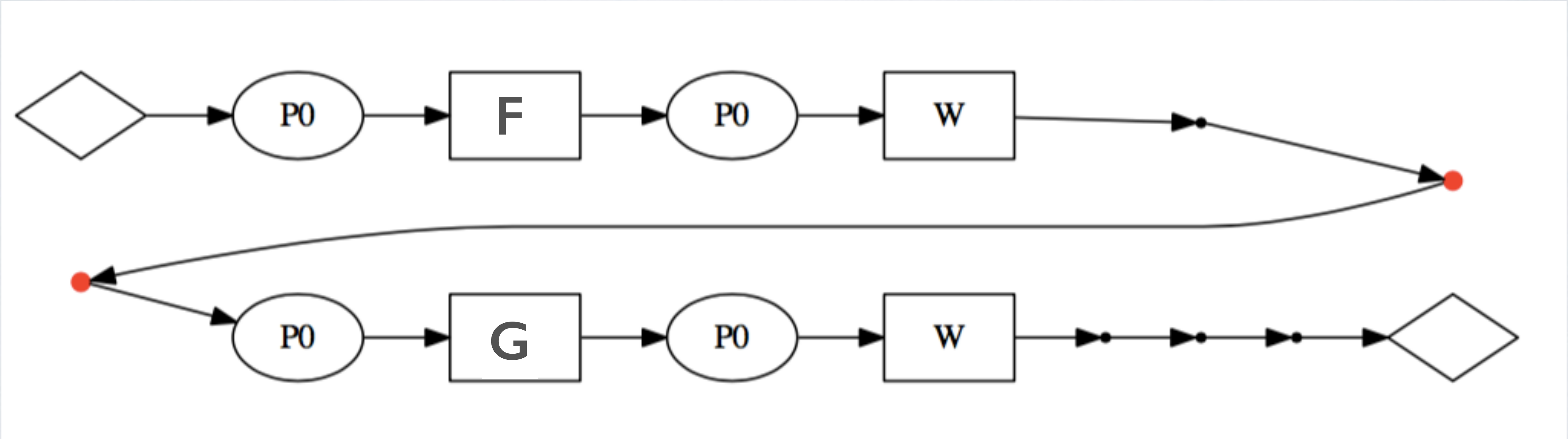

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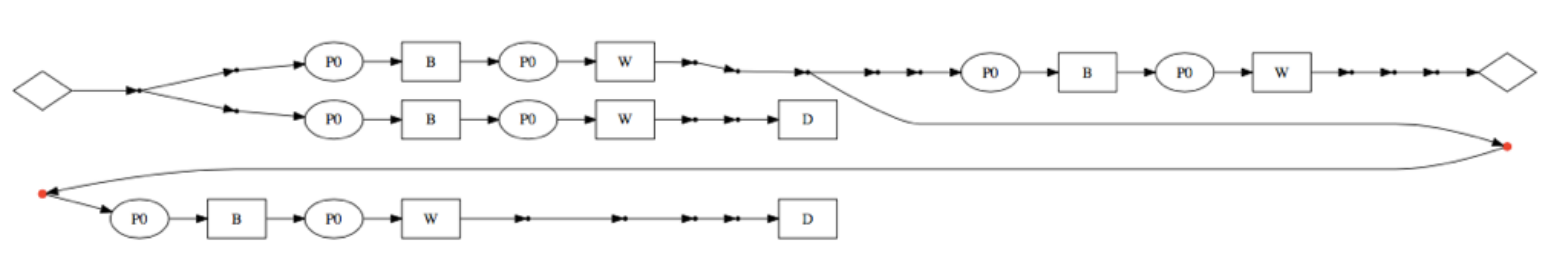

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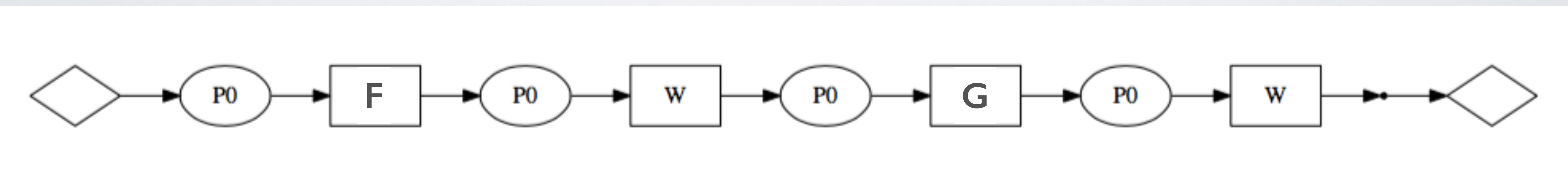
GRAPH REWRITE



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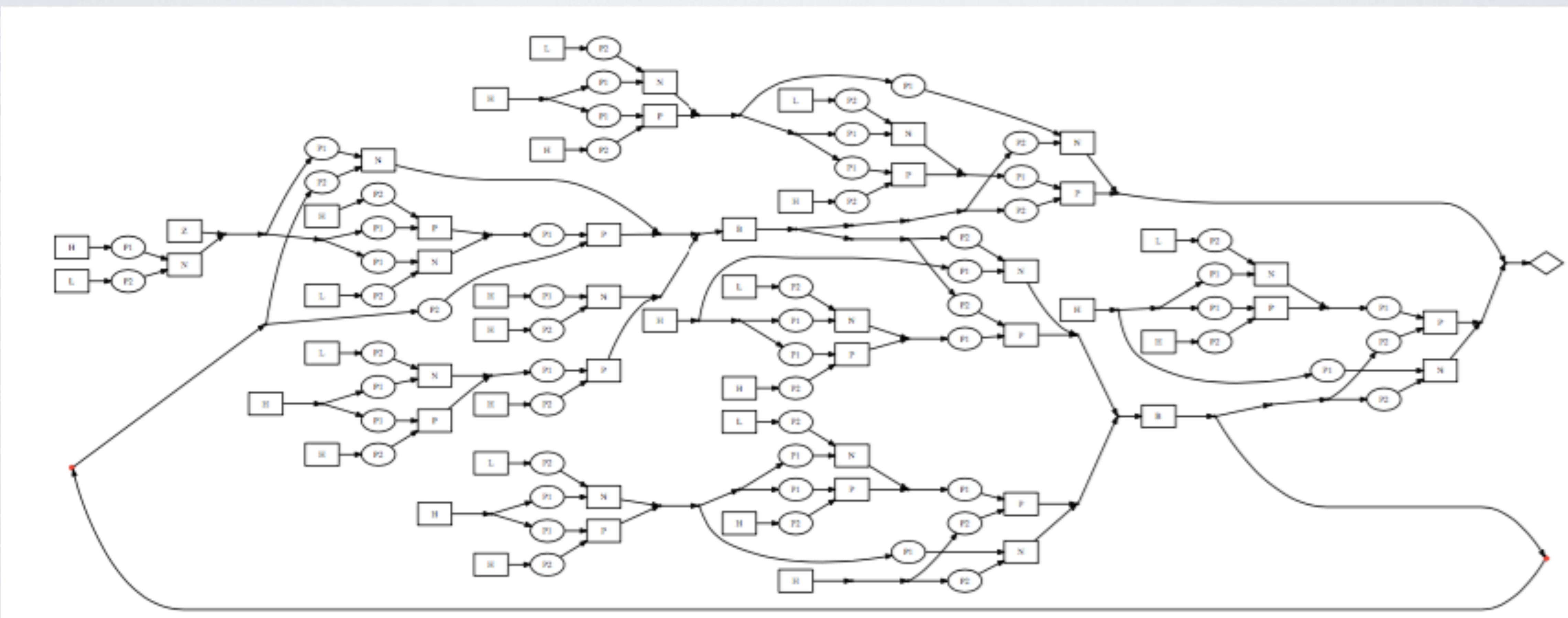
TRANSISTOR-LEVEL (MOSFET)



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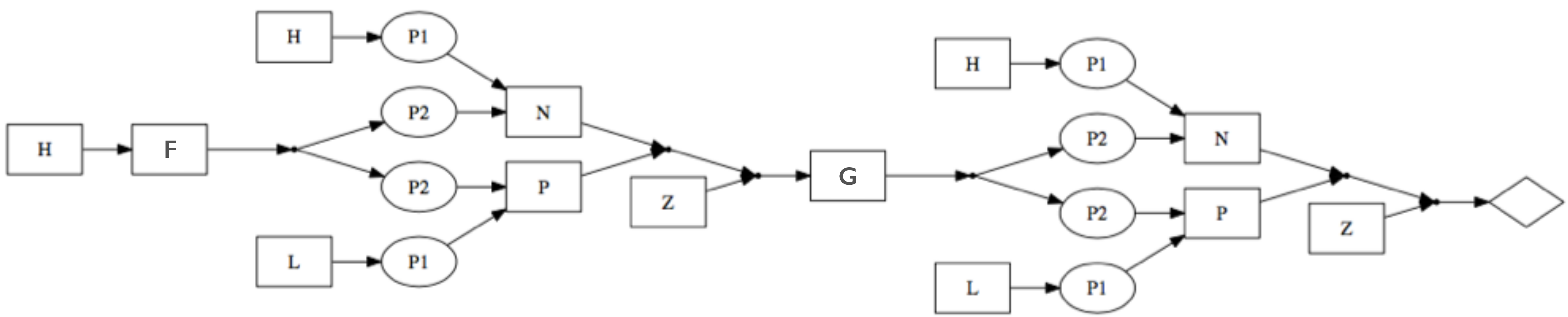

(submitted for publication)

RELATED WORK

- **HLS** : Sheeran, Luk, Singh
- **Semantics** : Mendler, Shiple, Berry
- **Diagrammatics** : Kissinger, Coecke, Abramsky
- **Systems** : Sobocinsky, Zanasi, Bronchi
- **Category theory** : Baez, Stay, Cazanescu, Stefanescu

CONCLUSION

- the interplay of **equations** and **diagrams**
- full automation of (partial) evaluation
- a new foundation for HW modelling
- compositional VHDL/Verilog